SEMICONDUCTOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-051637, filed March 16, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor memory device.

BACKGROUND

A NAND type flash memory in which memory cells are three-dimensionally arranged is known.

An example of related art includes JP-A-2012-227889.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a memory system that includes a semiconductor memory according to an embodiment.

FIG. 2 is a block diagram illustrating an example of an internal configuration of the semiconductor memory.

FIG. 3 is a diagram illustrating an example of an internal configuration of a memory cell array of the semiconductor memory.

FIG. 4 is a plan view illustrating an example of a structure of the memory cell array of the semiconductor memory.

FIG. 5 is a sectional view illustrating the example of the structure of the memory cell array of the semiconductor memory.

FIG. 6 is a diagram illustrating a relationship between data and a threshold voltage of the memory cell array.

FIG. 7 is a diagram illustrating a configuration example of the semiconductor memory according to a first embodiment.

FIG. 8 is a diagram illustrating a configuration example of a source line control circuit of the semiconductor memory according to the first embodiment.

FIG. 9 is a flowchart illustrating an operation example of the semiconductor memory according to the first embodiment.

FIG. 10 is a timing chart illustrating the operation example of the semiconductor memory according to the first embodiment.

FIG. 11 is a diagram illustrating the operation example of the semiconductor memory according to the first embodiment.

FIG. 12 is a diagram illustrating an operation example of the source line control circuit of the semiconductor memory according to the first embodiment.

FIG. 13 is a diagram illustrating a configuration example of a source line control circuit of a semiconductor memory according to a second embodiment.

FIG. 14 is a timing chart illustrating an operation example of a semiconductor memory according to a third embodiment.

FIG. 15 is a timing chart illustrating an operation example of a semiconductor memory according to a fourth embodiment.

FIG. 16 is a diagram illustrating a configuration example of a semiconductor memory according to a fifth embodiment.

FIG. 17 is a diagram illustrating a configuration example of a source line control circuit of a semiconductor memory according to the fifth embodiment.

DETAILED DESCRIPTION

The present embodiment now will be described more fully hereinafter with reference to the accompanying drawings, in which various embodiments are shown. In the drawings, the thickness of layers and regions may be exaggerated for clarity. Like numbers refer to like elements throughout. As used herein the term “and/or” includes any and all combinations of one or more of the associated listed items and may be abbreviated as “ / ”.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms “a,” “an” and “the” are intended to include the plurality of forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises,” “comprising,” “having,” “includes,” “including” and/or variations thereof, when used in this specification, specify the presence of stated features, regions, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, steps, operations, elements, components, and/or groups thereof.

It will be understood that when an element such as a layer or region is referred to as being “on” or extending “onto” another element (and/or variations thereof), it may be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or extending “directly onto” another element (and/or variations thereof), there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element (and/or variations thereof), it may be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element (and/or variations thereof), there are no intervening elements present.

It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, materials, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, material, region, layer or section from another element, material, region, layer or section. Thus, a first element, material, region, layer or section discussed below could be termed a second element, material, region, layer or section without departing from the teachings of the present invention.

Relative terms, such as “lower”, “back”, and “upper” may be used herein to describe one element's relationship to another element as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the structure in the Figure is turned over, elements described as being on the “backside” of substrate would then be oriented on “upper” surface of the substrate. The exemplary term “upper”, may therefore, encompasses both an orientation of “lower” and “upper,” depending on the particular orientation of the figure. Similarly, if the structure in one of the figures is turned over, elements described as “below” or “beneath” other elements would then be oriented “above” the other elements. The exemplary terms “below” or “beneath” can, therefore, encompass both an orientation of above and below.

Embodiments are described herein with reference to cross section and perspective illustrations that are schematic illustrations of idealized embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, a region illustrated or described as flat may, typically, have rough and/or nonlinear features. Moreover, sharp angles that are illustrated, typically, may be rounded. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region and are not intended to limit the scope of the present invention.

[0004]

Embodiments provide a semiconductor memory device which increases operational characteristics of a semiconductor memory.

[0005]

In general, according to one embodiment,

[0007]

Hereinafter, the present embodiments will be described in detail with reference to the drawings. In the following description, the same symbols or reference numerals will be attached to the elements having the same functions and configurations.

[0008]

In the following respective embodiments, if the reference numerals (for example, a word line WL, a bit line BL, various voltages and signals, or the like) accompanied by numbers or alphabetical characters for differentiation in the end are distinguished from each other, description in which the numbers in the end are omitted is used.

[0009]

Embodiments

A semiconductor memory device according to the embodiments will be described with reference to FIG. 1 to FIG. 18.

[0010]

(1) First Embodiment

A semiconductor memory (semiconductor memory device) according to a fist embodiment will be described with reference to FIG. 1 to FIG. 13.

[0011]

(a) Configuration Example

A configuration example of the semiconductor memory according to the fist embodiment will be described with reference to FIG. 1 to FIG. 8.

[0012]

As illustrated in FIG. 1, a memory system includes a storage device 1 and a host device 99.

[0013]

The host device 99 requests writing/erasing of data, and reading of data to the storage device 1.

The storage device 1 is coupled to the host device 99. The storage device 1 and the host device 99 perform data transfer to each other through, for example, a connector, wireless communication, the Internet, or the like.

[0014]

The storage device 1 includes a memory controller 200 and a semiconductor memory 201.

[0015]

The memory controller 200 includes a host interface circuit 210, an embedded memory (RAM) 220, a processor (CPU) 230, a buffer memory 240, a memory interface circuit 250, and an ECC circuit 260.

[0016]

The host interface circuit 210 couples the memory controller 200 to the host device 99. The host interface circuit 210 controls communication of the host device 99. Thus, the host interface circuit 210 transfers requests and data from the host device 99 to the CPU 230 and the buffer memory 240. The host interface circuit 210 transfers data stored in the buffer memory 240 to the host device 99, in response to a command of the CPU 230.

[0017]

The memory interface circuit 250 is connected to the semiconductor memory 201 via a bus. The memory interface circuit 250 controls communication of the semiconductor memory 201. The memory interface circuit 250 transfers a command from the CPU 230 to the semiconductor memory 201. When write data to the semiconductor memory 201, the memory interface circuit 250 transfers the data stored in the buffer memory 240 to the semiconductor memory 201. When read data from the semiconductor memory 201, the memory interface circuit 250 transfers the data from the semiconductor memory 201 to the buffer memory 240.

[0018]

The CPU 230 controls an operation of the whole of the memory controller 200. For example, when receiving a writing request from the host device 99, the CPU 230 issues a write command based on an interface standard. At the time of reading and erasing as well as writing, the CPU 230 issues a command according to the request of the host device 99. The CPU 230 performs various types of processing for managing the semiconductor memory 201, for example, wear leveling or the like. The CPU 230 performs various types of arithmetic, such as encryption processing of data or randomizing processing of data.

[0019]

The ECC circuit 260 performs error checking and correcting (ECC) processing of data. When write data the ECC circuit 260 generates parity based on the data to be written. When read data, the ECC circuit 260 detects error by generating syndrome from the parity. The ECC circuit 260 corrects the detected error. Meanwhile, the CPU 230 may have the function of the ECC circuit 260.

[0020]

The embedded memory 220 is a semiconductor memory such as a DRAM, and is used as a work memory (work area) of the CPU 230. The embedded memory 220 retains a firmware for managing the semiconductor memory 201, various management tables, or the like. The CPU 230 controls an operation of the semiconductor memory 201 with reference to information stored in the management table.

[0021]

The semiconductor memory 201 is a memory device that includes one or more memory chips embedded in a package. The semiconductor memory 201 is, for example, a NAND type flash memory. The storage device 1 (or memory system) including a flash memory is, for example, a memory card (for example, SDTM card), a USB memory, a solid state drive (SSD), or the like.

[0022]

As illustrated in FIG. 2, the flash memory 201 includes a memory cell array 11, and a plurality of circuits (hereinafter, is referred to as a peripheral circuit) that controls an operation of the memory cell array 11.

[0023]

For example, the NAND type flash memory 201 includes the memory cell array 11, a row decoder 12, a sense amplifier circuit 13, a source line control circuit 14, a well driver 15, a clamp circuit 16, a voltage generation circuit 17, a register 18, and a sequencer 19.

[0024]

The memory cell array 11 includes a plurality of blocks BK (BK0, BK1, BK2, …). The block BK is, for example, an erase unit of data. An erase operation according to the present embodiment is performed on a per block basis, but not limited to this. The erase operation may be performed on a per unit basis smaller than the block BLK. Such an erasing method is described in, for example, U.S. patent application No. 13/235389 filed September 18, 2011 and entitled “NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE”, and U.S. patent application No. 12/694690 filed January 27, 2010 and entitled “NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE”. The whole of the patent applications are incorporated in the present specification as a reference.

[0025]

Each of the block BK includes a plurality (for example, four) of string units SU (SU0, SU1, SU3, …). The plurality of string units (may be referred to as sub-blocks) SU is a plurality of NAND strings (memory cell units) 111. The NAND string 111 includes a plurality of memory cells that are connected in series to each other. The number of blocks included in the memory cell array 11, the number of string units included in one block BK, or the number of memory cells included in the NAND strings is arbitrary.

[0026]

The row decoder 12 decodes a block address and a page address, and selects one word line of a block corresponding to the address. The row decoder 12 applies voltages for operating the flash memory 201 to a selected word line and non-selected word lines.

[0027]

The sense amplifier circuit 13 senses and amplifies a signal that is output from the memory cell to a bit line, when read data. The sensed and amplified signal is treated as the data that is stored in the memory cell. In addition, the sense amplifier circuit 13 transfers a signal corresponding to the data (hereinafter, may be referred to as write data) to be written to the memory cells, when writing the data.

The clamp circuit 16 controls a potential of a bit line by controlling transistors included in the sense amplifier circuit 13.

[0028]

The source line control circuit 14 applies a voltage to a source line, and controls a potential of the source line.

The well driver 15 applies a voltage to a well region in which the NAND string 111 is provided.

[0029]

The voltage generation circuit 17 generates various voltages that are applied to each wire included in the flash memory 201.

[0030]

The register 18 can retains various signals. The register 18 retains, for example, a status of a write operation or an erase operation of the data. According to this, the flash memory 201 notifies the controller 200 of whether or not the operation is normally completed. The register 18 retains a command, an address, or the like that is received from the controller 200. The register 18 can retain various tables (management information).

[0031]

The sequencer 19 controls an operation of the whole of the flash memory 201. The sequencer 19 controls the operation of the flash memory 201, based on the control signals and commands which are transferred between the memory controller 200 and the flash memory 201.

[0032]

As illustrated in FIG. 3, the string unit SU includes four string groups SX (SX0 to SX3). Each string group SX includes a plurality of NAND strings 111.

[0033]

The NAND string 111 includes a plurality of memory cells MC (MC0 to MC(m-1)), and select transistors ST1 and ST2. Meanwhile, (m-1) is a natural number equal to or greater than “1”.

[0034]

The memory cell (memory cell transistor) MC includes a control gate and a charge accumulation layer (memory film). In the NAND string 111, the plurality of memory cells MC is connected in series to each other between the select transistors ST1 and ST2. One terminal (source or drain) of the memory cell MC(m-1) among the plurality of memory cells that are connected in series to each other, is connected to one terminal (source or drain) of the select transistor ST1. One terminal (source or drain) of the memory cell MC0 is connected to one terminal of the select transistor ST2.

[0035]

A plurality of select gate lines SGD0 to SGD3 are respectively connected to gates of the select transistors ST1 of a plurality of string groups SX0 to SX3.

One select gate line SGS is connected in common to gates of the select transistors ST2, between the plurality of string groups SX.

[0036]

The word lines WL0 to WL(m-1) are connected in common to control gates of the memory cells MC to which the same numbers as those of the word lines are attached, in the memory cells MC0 to MC(m-1) included in the same block BK.

[0037]

The word lines WL0 to WL(m-1) and the select gate line SGS are connected in common between the plurality of string groups SX0 to SX3 included in the same string unit SU. Select gate lines SGD are independently provided in each of the string groups SX0 to SX3, even in the same string unit SU.

[0038]

In the memory cell array 11, the other terminals (sources or drains) of the select transistors ST1 of the NAND string 111 of the same column, among the NAND strings 111 arranged in a matrix form, are connected in common to one bit line BL (BL0 to BL0n-1)) of a plurality of bit lines. The bit line BL is connected in common to the NAND strings 111, between the plurality of blocks BK. Meanwhile, (n-1) is a natural number equal to or greater than 1.

[0039]

The other terminal (source or drain) of the select transistor ST2 is connected to the source line SL.

[0040]

The reading and writing of the data is collectively performed with respect to the plurality of memory cells MC which is connected in common to any one of the word lines WL of a selected string group, in any one of the string units SU of any one of the blocks BK. The unit of the reading and writing of the data may be a page PG.

[0041]

As illustrated in an upper view of the memory cell array (block) of FIG. 4, a well contact CPWELL is provided in one terminal and the other terminal of the block BK in the X direction, in the block BK. For example, the block BK is provided in a region that is surrounded by the well contact CPWELL.

[0042]

A source line contact CELSRC is provided between the string units SU.

[0043]

The plurality of the NAND strings 111 includes semiconductor pillars 31 (311, 312). The semiconductor pillars 31 are arranged in the X direction and Y direction on a substrate (semiconductor region). Bit line contacts BC (BC1, BC2) are provided on the semiconductor pillars 31. The bit line contacts BC are connected to the bit lines BL.

[0044]

The two NAND strings 111 adjacent to each other in the Y direction are connected to the bit lines BL different from each other. In this case, the bit line contacts BC1 and BC2 are not arranged on the same straight line in parallel with each other in the Y direction in an X-Y plane. In the plurality of NAND strings 111 aligned in the Y direction, the positions of the bit line contacts BC1 and BC2 are alternately shifted in the X direction. The plurality of NAND strings 111 aligned in an oblique direction is connected to the bit lines BL different from each other.

[0045]

FIG. 5 illustrates a sectional structure taken along V-V line of FIG. 4. In Fig. 5, a member that is positioned in a depth direction (front direction) in a direction perpendicular to a paper surface, is denoted by a dotted line. In FIG. 5, one string unit SU is extracted and illustrated.

[0046]

As illustrated in FIG. 5, in the sectional structure of the memory cell array 11, a p type well region 20 is provided in a semiconductor region (for example, Si substrate).

[0047]

The semiconductor pillar s31 are provided on the p type well region 20. The semiconductor pillars 31 are extended in a direction approximately perpendicular to a surface of the p type well region 20 (substrate). A current flows through the semiconductor pillars 31. The semiconductor pillars 31 are regions in which channels of each transistor are formed, when the memory cells MC and the select transistors ST1 and ST2 operate.

[0048]

A memory film 29 is provided on a side surface of the semiconductor pillar 31. The memory film 29 includes a gate insulating film 291, a charge accumulation layer (insulating film) 292, and a block insulating film 293, sequentially from the semiconductor pillar 31 side.

[0049]

A plurality of conductive layers 23, 25, and 27 are laminated on the well region 20. An interlayer insulating film (not illustrated) is provided between the conductive layers 23, 25, and 27. The respective conductive layers (word lines) 23, 25, and 27 are provided on a side surface of the semiconductor pillar 31, via the memory film 29.

[0050]

A plurality (four, in the present example) of conductive layers 25 is connected to the select gate line SGD on the same drain side, in each of the NAND strings 111.

[0051]

A plurality (four, in the present example) of conductive layers 27 is connected to the select gate line SGS on the same source side.

[0052]

The bit line contact BC is provided on an upper end of the semiconductor pillar 31. A conductive layer (bit line) 32 is provided on the bit line contact.

[0053]

An n+ type diffusion layer 33 and a p+ type diffusion layer 34 are provided in a surface region of the well region 20.

[0054]

A source line contact CELSRC is provided on the diffusion layer 33. The source line contact CELSRC is connected to a source line SL. The source line SL is connected to the source line control circuit 14. The gate insulating film 291 covers a surface of the well region 20. The conductive layer 27 and the gate insulating film 291 are extended up to the vicinity of the diffusion layer 33. According to this, when the select transistor ST2 is turned on, the channel of the select transistor ST2 electrically connects the memory cell MC to the diffusion layer 33.

[0055]

Meanwhile, one source line SL may be provided in one block BK, and a plurality of source lines SL may be provided in one block BK. When the plurality of source lines SL is provided in one block BK, one source line is provided in one control unit (for example, string unit SU) in the block BK.

[0056]

A well contact PWELL is provided on a diffusion layer 34. The well contact CPWELL is connected to a well wire (not illustrated). The well wire is connected to a well driver 15. By applying a voltage to the well contact CPWELL, a voltage can be applied to the well region 20 and the semiconductor pillars 31.

[0057]

Meanwhile, in the present embodiment, a structure, an operation, and a fabrication method of a memory cell array with a three-dimensional structure employs configurations described in, for example, U.S. patent application No. 12/407,403 filed March 19, 2009 and entitled “THREE-DIMENSIONALLY STACKED NON-VOLATILE SEMICONDUCTOR MEMORY”, U.S. patent application No. 12/406,524 filed March 18, 2009 and entitled “THREE-DIMENSIONALLY STACKED NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE”, U.S. patent application No. 12/679,991 filed March 25, 2010 and entitled “NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND FABRICATION METHOD THEREOF”, and U.S. patent application No. 12/532,030 filed March 23, 2009 and entitled “SEMICONDUCTOR MEMORY AND FABRICATION METHOD THEREOF”.

[0058]

As illustrated in FIG. 6, in the flash memory 201, a threshold voltage of, for example, the memory cell MC belongs to any one of four threshold value distributions (erased state SE and programmed state SA, SB, and SC), in accordance with the data to be stored.

[0059]

A determination level (reading level) in which threshold value states (threshold value distributions) adjacent to each other are determined is each of voltage values VA, VB, and VC.

[0060]

When reading the data, the sequencer 19 applies a voltage including each reading level VA, VB, and VC to the selected word line. According to this, the memory cell in a threshold value state lower than the reading level is turned on, and the memory cell in a threshold value state higher than the reading level is turned off. Based on the result of ON and OFF of the memory cell MC, the data stored in the memory cell MC is determined.

[0061]

In a writing sequence of the flash memory, the sequencer 19 performs one or more writing loop. The writing loop includes a program step and a verification step.

[0062]

In the program step, the sequencer 19 applies a program voltage to the selected word line. The threshold voltage of the memory cell MC is shifted on a positive side.

[0063]

The sequencer 19 performs the verification step (program verification), after the program voltage is applied once.

[0064]

The sequencer 19 applies each of verification levels VAV, VBV, and VCV to the selected word line, and verifies the result of the program step. The sequencer 19 determines whether the memory cell is in a program-completed state (passed the verification) or in a program-uncompleted state (failed the verification), in accordance with ON or OFF of the memory cell MC according to the verification level.

[0065]

By repeating the program step and the verification step, the threshold voltage of the memory cell is shifted up to a target threshold voltage (threshold value distribution).

[0066]

Meanwhile, the memory cell acquires a threshold voltage of two values (one bit data), eight values (four bit data), or 16 values (eight bit data), according to characteristics or a type of the flash memory.

[0067]

At the time of reading the data and in the verification step, a cell current Icell flows through the NAND string 111 including a memory cell which is in an ON state. For example, the cell current Icell flows from the bit line BL toward the source line SL. A current Itotal which is the total of the cell current Icell becomes a current flowing through the source line SL. Meanwhile, there is also a case in which a small leakage current from the NAND string 111 including the memory cell that is in a ON state is included in the current Itotal flowing through the source line SL as a cell current.

For example, when the current Itotal is large, a voltage of the source line SL can be increased to a value greater than a set value to be controlled.

[0068]

The voltage of the source line SL is monitored in a wire (for example, top layer wire) on an upper layer side of the memory cell array. The NAND string 111 includes a parasitic resistance. Due to the parasitic resistance, a source voltage of the memory cell in the lower portion (semiconductor region side) of the NAND string can be different from the voltage of the source line SL to be monitored.

[0069]

The flash memory 201 (sequencer 19) according to the present embodiment monitors the current Itotal in the inside of the chip. The flash memory 201 controls the potential of the source line SL, based on the monitoring result.

The sequencer 19 determines a voltage to be applied to the source line SL (CELSRC), based on the monitoring result of the current Itotal and a magnitude of the resistance components of the NAND string 111, when the threshold voltage (potential of the bit line) of the memory cell MC is sensed. According to this, the sequencer 19 compensates for an increased amount of the voltage of the source line SL which is generated by the current Itotal.

[0070]

For example, the flash memory 201 offsets the increased amount of the voltage of the source line SL which is generated by the current Itotal, by decreasing a voltage that is applied to the source line SL by the source line control circuit 14 to a value smaller than the set value.

[0071]

For example, according to the source line control circuit 14 having the following circuit configuration, the flash memory 201 according to the present embodiment monitors the magnitude of the current Itotal, and controls the potential of the source line SL.

[0072]

(b) Configuration Example of Source Line Control Circuit

The source line control circuit 14 of the flash memory according to the present embodiment will be described with reference to FIG. 7 and FIG. 8.

[0073]

Firstly, a connection relationship between the source line control circuit 14 and other circuits will be described.

[0074]

As illustrated in FIG. 7, a sense amplifier circuit 13 includes a sense unit 131 and a transistor CT.

[0075]

Each bit line BL is connected to one sense unit 131 via the transistors CT (CT0 to CT(n-1)).

[0076]

A plurality of sense units 131 is connected in common to a voltage line (hereinafter, referred to as voltage line VHSA) to which a voltage VHSA is applied. The voltage VHSA is supplied to the sense unit 131.

[0077]

The transistor CT controls a potential of the bit line BL. Hereinafter, the transistor CT may be a clamp transistor CT. Gates of a plurality of clamp transistors are connected to a clamp circuit 16 via a common wire BLCLP.

[0078]

The clamp circuit 16 controls an output of the clamp transistor CT by controlling a potential of the wire BLCLP.

[0079]

The clamp circuit 16 includes a current source S1, a transistor TZ, and a resistor element R1.

One terminal (input terminal) of the current source S1 is connected to a terminal (hereinafter, referred to as a voltage terminal VDD) to which a power supply voltage VDD is applied. The other terminal (output terminal) of the current soured S1 is connected to the wire BLCLP.

One terminal of the transistor TZ (for example, n channel type field effect transistor) is connected to the wire BLCLP, and is connected to the other terminal of the current source S1. The other terminal of the transistor TZ is connected to one terminal of the resistor element R1. A gate of the transistor TZ is connected to one terminal of the transistor TZ. The transistor TZ is connected to a diode.

The other terminal of the resistor element R1 is connected to a terminal (hereinafter, referred to as a ground terminal Vss) to which a ground voltage Vss is applied.

[0080]

The clamp circuit 16 controls a potential of the wire BLCLP, based on a voltage between terminals of the resistor element R1.

For example, in the present embodiment, all the bit lines BL in the block are controlled in common. In the present embodiment, at the time of reading the data and at the time of the verification step, potentials of all bit lines BL in the string unit SU are controlled in common by the clamp circuit 16.

[0081]

The source line control circuit 14 is connected to the source line SL. The source line control circuit 14 controls the potential of the source line SL, based on a certain voltage value. The source line control circuit 14 includes a circuit (function) for monitoring the current Itotal.

[0082]

In the flash memory according to the present embodiment, the source line control circuit 14 includes a regulator circuit (voltage control circuit) 141, and a replica circuit (resistor replication circuit) 142.

[0083]

As illustrated in FIG. 8, the regulator circuit 141 is connected to the source line SL. The regulator circuit 141 controls a potential (hereinafter, may be referred to as a source line voltage) which is applied to the source line SL.

[0084]

The regulator circuit 141 includes an amplifier (for example, differential amplifier) A1 and a plurality of transistors T1 to T9.

[0085]

A first input terminal (inverting input terminal) IT1 of the amplifier A1 is connected to the source line SL. A second input terminal (non-inverting input terminal) IT2 of the amplifier A1 is connected to a plurality of transistors T1, T2, and T3. An output terminal OT of the amplifier A1 is connected to the transistor T4.

[0086]

The amplifier A1 outputs arithmetic results of a signal (voltage) that is supplied to the input terminals IT1 and IT2 from a third terminal (output terminal) OT as an output signal.

[0087]

A gate of the transistor (for example, n type field effect transistor) T1 is connected to the output terminal OT of the amplifier A1. One terminal of the transistor T1 is connected to a wire G\_source. One terminal of the transistor T1 is connected to a terminal (hereinafter, referred to as a voltage terminal VEXT) to which an external voltage VEXT is applied, via the transistor T2. The other terminal of the transistor T1 is connected to the ground terminal Vss.

[0088]

The wire G\_source is connected to one terminal of the transistor T1 and one terminal of the transistor T2.

A gate of the transistor (for example, p type field effect transistor) T2 receives a control signal PBIAS. ON and OFF of the transistor T2 are controlled by the control signal PBIAS. The transistor T2 that is in an ON state supplies the voltage VEXT to the wire G\_source.

[0089]

The transistor T1 is driven by an output signal from the amplifier A1. The transistor T1 outputs a drain current according to a magnitude of the output signal. A magnitude of the drain current of the transistor T1 is changed depending on the magnitude of the output signal of the amplifier A1. As the result, the transistor T1 controls the potential of the wire G\_source.

[0090]

A gate of the transistor T3 is connected to the wire G\_source. One terminal of the transistor T3 is connected to the terminal IT1 of the amplifier A1. The one terminal of the transistor T3 is connected to the voltage terminal VEXT, via the transistor T4. For example, the transistor T3 is an n type field effect transistor (n type high-voltage transistor) with a high insulating voltage (breakdown voltage).

[0091]

A gate of the transistor (for example, p type field effect transistor) T4 receives a control signal PLOAD. ON and OFF of the transistor T4 is controlled by the control signal PLOAD. The transistor T4 that is in an ON state supplies a voltage VEXT to one end of a current path of the transistor T4.

[0092]

The source line SL is connected to a junction of the transistor T3 and the transistor T4.

The transistor T3 outputs a drain current according to a potential of the wire G\_source. A magnitude of the drain current of the transistor T3 is changed depending on the potential of the wire G\_source. As the result, the voltage of the source line SL is controlled.

[0093]

A transistor T10 is an element that controls precharging of the input terminal IT1 of the amplifier A1 and the source line SL. One terminal of a transistor T10 is connected to the input terminal IT1. The other terminal of the transistor T10 is connected to the voltage terminal VEXT. A gate of the transistor T10 receives a control signal PRECH. ON and OFF of the transistor T10 is controlled by the control signal PRECH. According to this, each wire connected to the transistor T10 is precharged.

[0094]

The replica circuit 142 replicates a parasitic resistance included in the memory cell array 11.

The replica circuit 142 is connected to the regulator circuit 141 via the transistors T7, T8, and T9.

[0095]

The replica circuit 142 includes a resistor element RRP. Hereinafter, the resistor element RRP is referred to as a replica resistor element RRP, for the sake of clear explanation.

One terminal of the replica resistor element RRP is connected to a terminal (hereinafter, referred to as a voltage terminal VSRC) to which the voltage VSRC is applied. The voltage VSRC is applied to one terminal of the replica resistor element RRP.

[0096]

The replica resistor element RRP has a resistance value corresponding to a resistance component included in the NAND string 111. For example, a resistance value of the replica resistor element RRP corresponds to a total of various resistance values, such as a resistance value of a metal wire such as a bit line, a resistance value of a via plug (for example, via line contact), a resistance value of a semiconductor region (for example, the semiconductor pillar and the well region), and a resistance value of a source contact. The resistance value of the replica resistor element RRP is set, based on the results that are obtained from experimental results related to the flash memory, or logic values that are obtained from physical values of each material.

[0097]

Furthermore, the NAND string 111 includes an ON resistance of the select transistor ST2 on the source side, as a parasitic resistance.

The replica circuit 142 includes a plurality of transistors RT (RT0, RT1, RT2, RT3), in order to replicate the parasitic resistance caused by the select transistor ST2 on the source side. Hereinafter, for the sake of clear explanation, the transistor RT is referred to as a replica transistor.

[0098]

The replica transistors RT are connected in parallel with each other.

One terminal of the replica transistor RT is connected to the other terminal of the replica resistor element RRP, and the other terminal of the replica transistor RT is connected to one terminal of a transistor T8.

[0099]

Gates of the replica transistors RT0 to RT3 receive controls signals str (str0 to str3) different from each other. The replica transistors RT are turned on or off by the control signals str.

[0100]

Meanwhile, a NAND string (string group SX3) positioned in the vicinity of the source line contact CELSRC (source line SL), and a NAND string (string group SX0) positioned far from the source line SL, exist in the string unit SU (refer to FIG. 4 and FIG. 5).

In the plurality of the NAND strings 111, a magnitude of the ON resistance (parasitic resistance) of the select transistor ST2 on the source side is changed depending on a position of the NAND string 111 with respect to the source line contact CELSRC.

[0101]

When the select transistor ST2 on the source side is turned on, the NAND string 111 is connected to the source line contact CELSRC via a channel that is formed in the semiconductor region 20. A resistance value of the semiconductor region 20 between the select transistor ST2 on the source side and the source line contact CELSRC becomes a resistance component included in the NAND string.

A magnitude of a resistance is increased in proportion to a length of a semiconductor region. Hence, as the length of the semiconductor region between the select transistor ST2 on the source side and the source line contact CELSRC is lengthened, a resistance value that is included in the semiconductor region between the select transistor ST2 on the source side and the source line contact CELSRC is increased.

[0102]

For example, an ON resistance of the select transistor ST2 in the NAND string of the string group SX0 is larger than an ON resistance of the select transistor ST2 in the NAND string of the string group SX3.

[0103]

Thus, the ON resistance of the select transistor ST2 on the source side is changed depending on the position of the NAND string that is selected with respect to the source line contact CELSRC.

[0104]

For example, the replica transistor RT includes a plurality of transistors 9 that are connected in parallel with each other. The numbers of the transistors 9 included in the replica transistor RT are set differently in each of the replica transistors RT, in such a manner that the ON resistances of the select transistors ST2 on the source side which are different from each other can be replicated, in each string group SX.

[0105]

The source line control circuit 14 sets the replica transistor RT to an ON state in response to the control signal str, so as to correspond to a position (address of the select gate line SGD on the drain side) of the NAND string that is selected for writing or reading the data.

In this way, by using the replica transistor RT corresponding to the selected string, a difference of the ON resistance (parasitic resistance) of the select transistor on the source side in each NAND string is compensated.

[0106]

Furthermore, the replica transistor RT is provided on a substrate, in the same manner as the select transistor ST2 on the source side. Hence, the replica transistor RT can compensate for a change of the ON resistance of the select transistor ST2 which is generated by a change of an operational temperature.

[0107]

Meanwhile, only one resistor element RRP is illustrated in FIG. 8. However, the replica circuit 142 may include a plurality of resistor elements having resistance values different from each other. According to tested results of the flash memory, an element having a resistance value appropriate for controlling a source line voltage is selected from among a plurality of resistor elements. In addition, by connecting two or more resistor elements in parallel with each other or in series to each other, a replica resistor element RRP with a certain resistance value may be provided.

[0108]

A transistor T5 functions as an element (monitoring transistor) for monitoring the current Itotal flowing through the source line, in the replica circuit 142. For example, the transistor T5 is an n type field effect transistor (high-voltage transistor) with a high insulating voltage (breakdown voltage).

[0109]

One terminal of the transistor T5 is connected to the voltage terminal VSRC via the replica resistor element RRP and the replica transistor RT. The other terminal of the transistor T5 is connected to the ground terminal Vss. A junction (node) of the transistor T5 and the replica transistor RT becomes an output node ND1 of the replica circuit 142.

[0110]

Meanwhile, one terminal of the transistor T5 is connected to transistors T7 and T9 via the output node ND1.

[0111]

A gate of the transistor T5 is connected to the wire G\_source.

The transistor T5 is driven by a gate voltage, in common with the transistor T3. An output current (drain current) Imr of the transistor T5 is a mirror current of an output current (drain current) of the transistor T3.

[0112]

A gate size (for example, gate width) SZ2 of the transistor T5 is smaller than a gate size (for example, gate width) SZ1 of the transistor T3. For example, the gate size SZ2 of the transistor T5 is approximately one hundredth of the gate size SZ1 of the transistor T3. An output current of the transistor T5 becomes smaller than an output current of the transistor T3, according to a gate size ratio between the transistor T3 and the transistor T5. As the result, the replica circuit 142 can reduce a resistance value of a parasitic resistor which is replicated, according to the gate size ratio between the transistors T3 and T5. Thus, sizes of the resistor element RRP and the replica transistor RT can be reduced.

[0113]

As the transistor T5 operates, a current flows through the replica circuit 142. According to this current, a voltage is decreased by the resistor element RRP and the replica transistor RT.

The replica circuit 142 outputs a voltage VSRCz to which influence of the parasitic resistance (replica resistance of the NAND string) of the memory cell array 11 is reflected).

[0114]

In this way, a magnitude of the output voltage VSRCz of the replica circuit 142 is controlled by the transistor T5. The output voltage VSRCz is a voltage that is applied to the source line SL, when the voltage of the bit line BL is sensed at the time of determining the threshold voltage of the memory cell MC.

[0115]

Hereinafter, the replica resistor element RRP and the replica transistor RT are referred to as a replica element.

[0116]

Meanwhile, the replica circuit 142 may be provided by using the same structure (dummy string) as the NAND string, without using the replica resistor element and the replica transistor.

[0117]

The transistors (for example, n type field effect transistors) T6, T7, T8, and T9 are elements for selecting a signal (voltage) that is supplied to the input terminal IT2 of the amplifier A1. As any one of the transistors T6, T7, and T8 enters an ON state, a signal (voltage) that is supplied to the input terminal of the amplifier A1 can be selected.

[0118]

A gate of the transistor T6 receives a control signal SW1. ON and OFF of the transistor T6 is controlled by the control signal SW1.

[0119]

When turned on, the transistor T6 supplies the voltage VSRC from the voltage generation circuit 17 to the terminal IT2 of the amplifier A1. The voltage VSRC is, for example, approximately 0.8 V.

[0120]

A gate of the transistor T7 receives a control signal SW2. ON and OFF of the transistor T7 is controlled by the control signal SW2. The transistor T7 is connected between a terminal IT2 of the amplifier A1 and the output node ND1.

[0121]

When turned on, the transistor T7 supplies the output voltage VSRCz from the replica circuit 142 to the output terminal IT2 of the amplifier A1.

[0122]

A gate of the transistor T8 receives a control signal SW3. ON and OFF of the transistor T8 is controlled by the control signal SW3.

When turned on, the transistor T8 supplies a voltage retained in a capacitor C1 to the terminal IT2 of the amplifier A1.

[0123]

One terminal of the transistor T9 is connected to the one terminal of the transistor T5 and the other terminal of the transistor T7. A junction of the other terminal of the transistor T9 and the other terminal of transistor T8 is connected to one terminal of the capacitor C1. The other terminal of the capacitor C1 is grounded. A gate of the transistor T9 receives a control signal SW4. ON and OFF of the transistor T9 is controlled by the control signal SW4. The capacitor C1 retains the output signal VSRC of the replica circuit 142 via the transistor T9 that is in an ON state.

[0124]

The regulator circuit 141 operates, in such a manner that a voltage which is applied to the source line SL becomes approximately the voltages VSRC and VSRCz which are supplied to the input terminal IT2 of the amplifier A1.

[0125]

In the flash memory according to the present embodiment, according to the following operation, the source line control circuit 14 controls using voltages that are supplied from each of the transistors T1 to T3 source line voltage, based on the monitoring result of a current flowing through the source line.

[0126]

(c) Operation Example

An operation example (method of controlling a semiconductor memory and a memory controller) of a memory system including a semiconductor memory according to the present embodiment will be described with reference to FIG. 9 and FIG. 10.

Here, FIG. 1 to FIG. 8 will also be used as references. Meanwhile, a potential of the wire CELSRC of FIG. 10 indicates a voltage which is applied to the source line (source line contact) by the source line control circuit 14.

[0127]

Determination of a threshold voltage of the memory cell MC is performed in the verification step in a writing sequence, or at the time of read data in a reading sequence.

Hereinafter, a method of controlling a potential of the source line of the flash memory according to the present embodiment will be described by using the verification step (verification operation) of a multi-value flash memory (here, flash memory of four values) as an example.

[0128]

As illustrated in a flowchart of FIG. 9, at the time of writing the data, the memory controller 200 transmits a write command, an address for data writing, and data from the host device 99 to the flash memory 201 (step ST100).

[0129]

The flash memory 201 receives a command from the memory controller 200 (step ST0). The sequencer 19 in the flash memory 201 interprets the command, and starts an operation sequence, based on the command.

[0130]

When the command is a write command, the sequencer 19 executes a program step (step ST1). The sequencer 19 applies a program voltage to a selected word line that is indicated by an address.

[0131]

After the program voltage is applied, the sequencer 19 starts determination (verification step) of the threshold voltage of the memory cell MC in a certain level, as illustrated in a timing chart (diagram illustrating potentials of each wire and a change of the control signal) of FIG. 10 (step ST2).

The voltage generation circuit 17 generates various voltages (for example, the voltage VSRC and the voltage VHSA), according to the control of the sequencer 19. The well driver 15 applies a voltage to the well region 20 via the well wire and well contact CPWELL.

[0132]

The voltage VHSA is applied to the sense unit 131 of the sense amplifier circuit 13.

In addition, the clamp circuit 16 controls the voltage of the wire BLCLP, and applies the voltage VCLP to the gate of the clamp transistor CT. According to this, the sense amplifier circuit 13 applies the voltage VCLP-Vt to the plurality of bit lines (for example, all the bit lines) BL in the selected string unit SU, using the clamp transistor CT. Vt is a threshold voltage of a clamp transistor.

The row decoder 12 selects the block BK, the string unit SU, the string group, and the page PG that are indicated by the address.

[0133]

The source line control circuit 14 applies various voltages to the source line SL and each wire (terminal) in the source line control circuit 14.

[0134]

For example, the source line control circuit 14 sets the control signal PRECH to an L level, and precharges the source line SL and the input terminal IT1 of the amplifier A1, according to the control of the sequencer 19. After precharging, the source line control circuit 14 sets the control signal PRECH to an H level. Thereafter, the source line control circuit 14 sets the control signal PBAIS and the control signal PLOAD to an L level, and applies the voltage VEXT to each wire.

[0135]

According to this, the source line control circuit 14 enters a state in which the control of the source line voltage CELSRC and the monitoring of the current Itotal can be started. The source line control circuit 14 applies the voltage VSRC to the source line SL, as an initial state of verification.

[0136]

The row decoder 12 applies the non-select voltage Vread to the non-selected word lines, and applies the verification voltage VVF to the selected word line. In the memory cell of four values, for example, the verification voltage VVF includes three verification levels (determination voltage values) VAV, VBV, and VCV. According to this, the sequencer 19 performs verification of each step in a sequence of A step, B step, and C step.

[0137]

The sequencer 19 sets the voltage value of the verification voltage VVF to the verification level VAV, and performs program verification related to the A step. By applying the verification level VAV, the memory cell MC is turned on or off according to the threshold state of the memory cell MC.

[0138]

During a verification period (hereinafter, the verification period is referred to as a verification step) of an A state, the memory cell MC with a threshold voltage equal to or lower than the verification level VAV is turned on, and the memory cell with a threshold voltage higher than the verification level VAV is turned off. The memory cell that is turned on by the verification level VAV is a memory cell of failed verification with regard to the A state. The memory cell that is turned off by the verification level VAV is a memory cell of failed verification with regard to the A state.

[0139]

The cell current Icell flows through the NAND string 111 that includes a memory cell in an ON state.

The cell current Icell is supplied to the source line SL. A current (and a leakage current) which is the total of the cell current Icell flows through the source line SL as the current Itoal.

[0140]

In the present embodiment, during a first period (hereinafter, referred to as a monitoring period) d1 after verification starts, the source line control circuit 14 monitors a magnitude of the current Itotal of the voltage VSRC, in parallel to the program verification (step ST3).

The source line control circuit 14 (or the sequencer 19) sets the control signal SW1 to an H level, during the monitoring period d1. In addition, during the monitoring period d1, the source line control circuit 14 sets the control signals SW2, SW3, and SE4 to an L level.

According to this, the transistor T1 is turned on, and supplies the voltage VSRC to the terminal IT2 of the amplifier A1.

[0141]

In the regulator circuit 141, the amplifier A1 performs a differential amplification (comparison) of the voltage of the source line SL supplied to the terminal IT1 and the voltage VSRC supplied to the terminal IT2. The amplifier A1 outputs a signal (for example, signal of an L level or an H level) which is obtained by performing a differential amplification, to the gate of the transistor T1 from the output terminal OT.

[0142]

For example, when a voltage (voltage of the source line) which is applied to the input terminal IT1 is higher than the voltage VSRC which is applied to the input terminal IT2, the amplifier A1 outputs a signal of an L level. The transistor T1 is turned off by the signal of an L level from the amplifier A1. The voltage of the wire G\_source is maintained in a charged state, and is set to approximately the voltage VEXT.

The transistor T3 operates in accordance with the voltage of the wire G\_source in a charged state. As the result, the current Itotal flows into the ground terminal Vss by the transistor T3.

[0143]

In this way, when the voltage of the source line SL is higher than the reference voltage VSRC, the source line control circuit 14 increases a current amount that is output from the source line SL, and decreases the voltage of the source line SL.

[0144]

For example, when the voltage of the source line SL that is applied to the input terminal IT1 is equal to or lower than the voltage VSRC that is applied to the input terminal IT2, the amplifier A1 outputs a signal of an H level (or a signal of a certain voltage between an L level and an H level).

[0145]

The transistor T1 is turned on by a signal of an H level from the amplifier A1. According to this, the wire G\_source is discharged, and the voltage of the wire G\_source is decreased to a voltage lower than the voltage VEXT by the discharging.

[0146]

The transistor T3 operates according to the voltage of the wire G\_source. When the voltage of the wire G\_source is lower than the voltage VEXT, the drain current of the transistor T3 is decreased to a current lower than the drain current of the transistor T3 when the voltage VEXT is applied to the gate of the transistor T3. Hence, in-take of the current Itotal performed by the transistor T3 is weak. As the result, the source line SL is hardly discharged.

[0147]

In this way, when the voltage of the source line SL is equal to or lower than the reference voltage VSRC, the source line control circuit 14 decreases a current amount that is discharged from the source line SL, and increases the voltage of the source line SL.

[0148]

The operation of the regulator circuit 141 is repeated during the monitoring period d1, and thereby a voltage that is applied to the source line SL is controlled so as to become a certain value VSRC.

[0149]

During the monitoring period d1, the transistor T5 controls a magnitude of the output voltage VSRCz of the replica circuit 142, in parallel to the control of the voltage of the source line SL using the voltage VSRC which is performed by the amplifier A1. Hereinafter, the voltage VSRCz is referred to as a correction voltage VSRCz.

[0150]

As described above, the gate of the transistor T5 is connected to the wire G\_source. The transistor T5 is driven by a gate voltage having the same magnitude as that of the transistor T3. Hence, the transistor T5 outputs the mirror current Imr corresponding to the drain current of the transistor T3. A current flows through the replica elements RRP and RT, and thereby voltage drop of the voltage VSRC occurs. According to this, the correction voltage VSRCz is generated in the node ND1.

[0151]

During the monitoring period d1, a magnitude of the mirror current Imr is changed in conjunction with adjustment of the current Itotal. According to this, a magnitude of a current flowing through the replica resistor element RRP and the replica transistor RT (replica element) is changed. As the result, a magnitude of the correction voltage VSRCz of the node ND1 is changed.

[0152]

For example, if the mirror current Imr increases, the currents flowing through the replica elements RRP and RT increase. According to this, an amount of voltage drop caused by the replica elements RRP and RT is increased. As the result, the voltage VSRCz of the output node ND1 decreases. If the mirror current Imr decreases, the currents flowing through the replica elements RRP and RT decrease. According to this, an amount of voltage drop caused by the replica elements RRP and RT is decreased. As the result, the voltage VSRCz of the output node ND1 increases.

[0153]

In the present embodiment, the replica transistor RT corresponding to a select string group (NAND string), among the plurality of replica transistors RT0, is turned on by the control signal str. According to this, an ON resistance of the select transistor ST2 on the source side in which a gap (length of the semiconductor region between the source line contact CELSRC and the NAND string) between the source line contact CELSRC and the NAND string is taken into account, is reflected to an amount of drop of the correction voltage VSRCz of the replica circuit 142.

[0154]

As described above, the source line control circuit 14 generates the voltage VSRCz that is adjusted based on the monitoring result (a floating amount of the voltage of the source line SL) of the current Itotal and the parasitic resistance of the memory cell array, using the replica circuit 142, under the control of the sequencer 19. According to this, a voltage in which a floating amount of the voltage of the source line SL that is generated by the current Itotal is offset, is generated. For example, the correction voltage VSRCz is lower than the reference voltage VSRC (for example, 0.8 V).

[0155]

As illustrated in FIG. 10, after the monitoring period (adjusting period of the compensation voltage value) d1 of the current Itotal is completed, the source line control circuit 14 makes a signal level of the control signal SW1 be transitioned from an H level to an L level. The source line control circuit 14 sets the control signal SW2 to an H level, in synchronization with a timing in which the control signal SW1 is set to an L level. The transistor T6 is turned off, and the transistor T7 is turned on. A voltage that is supplied to the input terminal IT2 of the amplifier A1 is switched to the correction voltage VSRCz from the reference voltage VSRC (step ST4).

[0156]

During a sensing period d2, the transistor T7 is maintained in an ON state, and the transistor T7 supplies the correction voltage VSRCz to which a change of the current Itotal occurring in the sensing period d2 is reflected, to the amplifier A1. According to this, accuracy of the determination of the threshold voltage of the memory cell is increased.

[0157]

Meanwhile, the monitoring results of the current Itotal may be reflected to a control of the potential of the well region 20.

[0158]

As illustrated in FIG. 9 and FIG. 10, during the sensing period d2 after the monitoring period d1, the regulator circuit 141 controls a magnitude of the source line voltage CELSRC, based on the results of arithmetic processing of the correction voltage VSRCz and the voltage of the source line SL (step ST3). According to this, the source line control circuit 14 controls the voltage of the source line CELSRC, in such a manner that a voltage which is applied to the source line (source line contact) CELSRC becomes the voltage CSRCz (VSRCz<VSRC). For example, a total of the correction voltage VSRCz and a floating amount of the voltage of the source line SL is approximately 0.8 V.

[0159]

In a verification stage of the A state, the voltage of the source line SL is controlled by using a correction voltage VSRCz-a, and thereby a gate-source voltage Vgs and a drain-source voltage Vds which are affected by a parasitic resistance, are compensated.

[0160]

At a time x1 of the sensing period d2, the sense unit 131 senses the voltage of the bit line BL (step ST5). According to this, a latch circuit (not illustrated) in the sense amplifier circuit 13 receives the results of the verification of the A state.

[0161]

After the verification of the A state, a verification stage DB of the B state and a verification stage DC of the C state are sequentially implemented.

[0162]

In the present operation example, at the time of implementing (switching of verification level) of the verification stage, a control (first processing) of the voltage of the bit line BL according to an ON or OFF state of the memory cell MC is performed.

For example, when the verification level is switched from the level VAV to the level VBV, the sense amplifier circuit 13 sets the voltage of the bit line BL to the same voltage as the source line SL, without charging the bit line BL that is connected to the memory cell (memory cell of passed verification with regard to the A state) in an OFF state. According to this, the bit line BL that is connected to the memory cell in an OFF state enters a non-select state.

Hereinafter, an operation of setting the bit line to a non-select state based on the determination results (for example, verification results) of the threshold voltage of the memory cell MC, is referred to as lock out processing LCK.

[0163]

By the lock out processing LCK, the cell current Icell is hardly generated, in the NAND string that is connected to the bit line BL in a non-select state.

In this way, since the cell current Icell from the bit line (NAND string including the memory cells) in which the lock out processing is completed is reduced, a current value of the current Itotal in which the lock out processing is completed is less than a current value of the current Itotal in which the lock out processing is not performed.

[0164]

In the verification stages DB and DC of the B state and the C state, the source line control circuit 14 monitors the current Itotal during the motoring period d1, in substantially the same manner as the voltage control of the source line SL in the verification stage DA of the A state (step ST2). The source line control circuit 14 controls the voltage of the source line SL, based on the monitoring results during the sensing period d2 (step ST3). Thereafter, the voltage of the bit line BL is sensed by the sense amplifier circuit 13 (step ST4).

[0165]

When the lock out processing LCK is performed at the time of program verification, the verification level is increased, and thereby the current Itotal is reduced.

[0166]

By the reduction of the current Itotal (reduction of the reduction current Icell), a floating amount of the voltage of the source line SL at the time of verification of the C state is less than a floating amount of the voltage of the source line SL at the time of verification of the A state.

[0167]

In the present embodiment, the mirror current Imr of the transistor T5 decreases, and in contrast to this, the correction voltage VSRCz increases. In this way, the source line control circuit 14 compensates for a change of the floating amount of the source line SL due to the decrease of the current Itotal.

[0168]

Thus, as in the present embodiment, when the lock out processing LCK is performed, a correction voltage VSRCz-c at the time of verification of the C state is higher than a correction voltage VSRCz-a at the time of verification of the A state. In addition, a correction voltage VSRCz-b at the time of verification of the B state is equal to or higher than the correction voltage VSRCz-a, and is equal to or lower than the correction voltage VSRCz-c.

[0169]

In this way, the source line control circuit 14 can apply a large potential in which the floating amount of the voltage of the source line SL is taken into account, to the source line SL in each verification stage, in such a manner that the verification is performed in a state in which the voltages of the source lines SL are the same as each other, even if the verification level is changed.

[0170]

As described above, the flash memory according to the present embodiment sequentially performs the A state, the B state, and the C state, in the verification step.

[0171]

The sequencer 19 determines whether or not the verification results of all the cells selected as writing targets are pass (step ST6).

[0172]

When the verification results of all the select cells are not pass, the sequencer 19 repeats a writing loop (steps ST1 to ST6) including the program step and the verification step until writing of data to be stored in each memory cell is completed (until verification of all the memory cells are pass).

When the verification results of all the select cells are pass, the sequencer 19 completes a writing sequence. The sequencer 19 notifies the memory controller that the writing sequence is completed (step ST7).

[0173]

The controller 200 receives notification of completion of the writing sequence from the flash memory 200 (step ST109). According to this, the controller 200 senses completion of the sequence of the flash memory corresponding to a command.

[0174]

By the operation described above, operations of the flash memory and the memory system according to the present embodiment are completed.

[0175]

Meanwhile, in the flash memory according to the present embodiment, the control of the voltage of the source line based on the monitoring results of the current flowing through the source line SL described above, can be applied to a read operation of the flash memory.

[0176]

As illustrated in FIG. 11, the control of the source line voltage at the time of data reading based on a read command from the memory controller 200, is substantially the same as the control of the source line voltage CELSRC at the time of verification, because magnitudes of the reading levels VA, VB, and VC of a voltage VCGRV that is applied to the selected word line, and a sequence to be applied are different from each other.

[0177]

Meanwhile, in the example described above, in the stages of each state, the flash memory determines whether the memory cell is in an ON state or an OFF state (a voltage state of the bit line BL) by performing the sensing operation once. However, there is a possibility that, if the current Itotal is increased, the threshold value distribution of the memory cells is spread due to the floating of the source line SL. For this reason, there is a possibility that the flash memory cannot correctly determine ON and OFF of the memory cell by performing the sense operation once, in each stage. Hence, the flash memory may perform the sensing operation of two times in each stage.

[0178]

(d) Modification Example

In the flash memory according to the present embodiment, the source line control circuit 14 can provide a correction voltage during the sensing period, using the capacitor C1.

[0179]

As illustrated in FIG. 12, the source line control circuit 14 supplies the voltage VSRC to the input terminal IT1 of the amplifier A1, in response to the control signal SW1 of an H level, during the monitoring period d1, in the same manner as in the operation example of the source line control circuit 14 illustrated in FIG. 10. The amplifier A1 outputs a result in which the voltage of the source line SL and the voltage VSRC are compared to each other, from the output terminal OT. The respective transistors T1, T3, and T5 operate.

[0180]

The source line control circuit 14 sets the control signal SW4 to an H level, during the monitoring period d1. According to this, the transistor T9 is turned on, and the capacitor C1 is connected to the replica circuit 142.

[0181]

The correction voltage VSRCz according to a drive state (magnitude of the current Itotal) of the transistor T5 is applied to the capacitor C1 via the transistor T9 in an ON state. According to this, the capacitor C1 is charged.

[0182]

The source line control circuit 14 transitions a signal level of the control signal SW4 to an L level from an H level, at a timing in which a signal level of the control signal SW1 is set to an L level. By the transistor T9 in an OFF state, a voltage which is applied to the capacitor C1 from the replica circuit 142 is blocked.

[0183]

The source line control circuit 14 transitions a signal level of the control signal SW3 to an H level from an L level, in synchronization with a timing in which the control signal SW4 is set to an L level. According to this, the transistor T8 is turned on, and the capacitor C1 is connected to the amplifier A1.

[0184]

A voltage according to charges accumulated in the capacitor C1 is supplied to the terminal IT2 of the amplifier A1, as a voltage value (source line voltage) during the sensing period d2. The voltage of the capacitor C1 corresponds to the correction voltage VSRCz during the monitoring period d1.

[0185]

In a state in which the capacitor C1 is connected to the amplifier A1, a voltage state of the bit line BL is sensed. Thereafter, the source line control circuit 14 transitions a signal level of the control signal SW3 to an L level from an H level. According to this, the capacitor C1 is electrically disconnected from the amplifier A1.

[0186]

In this way, the control of the source line voltage is completed during the determination period of the threshold voltage of the memory cell MC with regard to a certain state.

[0187]

As described in the present modification example, when the correction voltage VSRCz is supplied by the voltage of the capacitor C1, the flash memory 201 according to the present embodiment can electrically disconnect the replica circuit 142 from the amplifier A1. As the result, the flash memory 201 according to the present embodiment can deactivate the replica circuit 142, and can reduce power consumption caused by the replica circuit 142.

[0188]

(e) Summary

The flash memory according to the present embodiment monitors a total (current flowing through the source line) of the cell currents, in the inside of the chip, at the time of determining the threshold voltage of the memory cell.

The flash memory according to the present embodiment feeds back the monitoring results to the control of the voltage of the source line.

[0189]

According to this, the flash memory according to the present embodiment compensates for the floating of the source line caused by the cell current.

AS the result, the flash memory according to the present embodiment can suppress data pattern dependency (threshold voltage dependency) of the memory cell on the gate-source voltage and the drain-source voltage of the memory cell.

[0190]

Thus, the flash memory according to the present embodiment can suppress spreading of the threshold value distribution width of the memory caused by the noise of the source line, and can improve characteristics of the memory cell.

[0191]

In addition, the flash memory according to the present embodiment can suppress an increase in a chip size caused by an increase of the number of source line contacts and high frequency of shunt.

[0192]

Furthermore, as described in the present embodiment, when the voltage (a source voltage of the memory cell) of the source line SL is suppressed, both of the gate-source voltage Vgs and the drain-source voltage Vds are simultaneously adjusted. Furthermore, an RC time constant of the source line is smaller by one digit than RC time constants of the word line and the bit line. Hence, the flash memory according to the present embodiment can reduce the period for correcting the gate-source voltage Vgs and the drain-source voltage Vds of the flash memory.

[0193]

As the result, the flash memory according to the present embodiment can suppress a delay of the operation, and can improve reliability of the operation.

[0194]

As described above, the flash memory according to the present embodiment can improve operating characteristics.

[0195]

(2) Second Embodiment

A semiconductor memory device according to the second embodiment will be described with reference to FIG. 13.

[0196]

In the flash memory according to the present embodiment, the source line control circuit 14 may suppress a voltage that is applied to the source line, using a digital value of a voltage value based on the monitoring results of the current flowing through the source line.

[0197]

As illustrated in FIG. 13, the source line control circuit 14 includes an analog-digital conversion circuit (ADC circuit) 145.

[0198]

The ADC circuit 145 converts the correction voltage VSRCz to a digital value from an analog value. The ADC circuit 145 feeds back the digital voltage value DVSRCz to the voltage generation circuit 17 as a DAC value for controlling a reference voltage value of the amplifier A1.

[0199]

A generation unit 170 of the voltage generation circuit 17 generates a reference voltage value (voltage that is applied to the source line) of the amplifier A1.

The generation unit 170 supplies the voltage VSRC to the regulator circuit 141, during the monitoring period d1.

The generation unit 170 changes a magnitude of an output voltage VSRCx, based on a DAC value SVSRCz. The generation unit 170 supplies the voltage VSRCz that is modulated based on the DAC value to the regulator circuit 141.

[0200]

The regulator circuit 141 controls a magnitude of the source line voltage CELSRC, using the reference voltage VSRCz, in such a manner that the voltage VSRCz which is controlled based on the DAC vale DVSRCz is applied to the source line CELSRC.

[0201]

In this way, in the present embodiment, the source line control circuit 14 performs substantially the same operation as the operation described in the first embodiment, using the correction voltage VSRCz that is adjusted by a digital value.

[0202]

As described above, even when the voltage that is used for the source line control circuit 14 is controlled by using the digital value, the flash memory according to the present embodiment obtains the same effect as the flash memory according to the first embodiment.

[0203]

(3) Third Embodiment

A semiconductor memory device according to a third embodiment will be described with reference to FIG. 14.

[0204]

The flash memory according to the third embodiment is different from the flash memories according to the first and second embodiments in a method of controlling the voltage of the bit line, at the time of determining the threshold voltage of the memory cell.

[0205]

In the flash memory according to the present embodiment, during the second processing for the bit line, the sense amplifier circuit (sense unit) continuously charges the bit line BL, regardless of the determination result (ON or OFF state of the memory cell) of the threshold voltage of the memory cell.

That is, the second processing is a control method of the bit line in which the lock out processing is not performed.

[0206]

In the following description, the second processing in which the lock out processing is not performed is referred to as no lock out processing.

[0207]

When the flash memory according to the present embodiment performs a verification step (or data reading) using no lock out processing, the sense amplifier circuit 13 charges not only the bit line BL connected to the memory cell in an ON state, but also the bit line BL connected to the memory cell in an OFF state, at the time of verification of a certain state.

[0208]

The flash memory according to the present embodiment performs determination (verification or data reading) of the threshold voltage of the memory cell, as described below.

[0209]

As illustrated in a figure illustrating an operation of the flash memory in FIG. 14, the flash memory according to the present embodiment controls a potential of a wire in the memory cell array, in the same manner as the operation illustrated in FIG. 9, for example, at the time of verification step.

[0210]

For example, during the monitoring period d1 of the verification stage of the A state, the source line control circuit 14 monitors the current Itotal by using the voltage Vsrc as a reference voltage.

[0211]

During the sensing period d2, the source line control circuit 14 senses the voltage (ON or OFF of the memory cell MC) of the bit line BL, in a state in which the voltage of the source line SL is controlled by using the correction voltage VSRCz based on the monitoring results as a reference.

[0212]

When verification is transitioned from the A state to the B state, the sense amplifier circuit 13 charges not only the bit line BL connected to the memory cell in an ON state, but also the bit line BL connected to the memory cell in an OFF state, regardless of the verification results of the memory cell with regard to the A state. In the B state, various types of processing are performed during the monitoring period and the sensing period, in a state in which all the bit lines BL are charged.

[0213]

Even when verification is transitioned from the B state to the C state, the lock out processing is not performed, and the sense amplifier circuit 13 charges all the bit lines BL in the select string unit (select block).

[0214]

In this way, the flash memory according to the present embodiment continuously charges all the bit lines BL connected to the memory cells that are verification targets, during the verification step.

Hence, in the flash memory in which no lock out processing is performed in the same manner as in the present embodiment, reduction of the current Icell caused by the bit line BL that is set to a non-select state, does not occur.

[0215]

In the flash memory of no lock out processing, as the verification level becomes higher, the number of memory cell to be turned on is increased. As the result, with the progress of the stage during the verification step, the number of NAND strings in which the cell current Icell is generated is increased.

[0216]

As the result, the flash memory to which the no lock out processing is applied has a tendency in which an amount of currents flowing through the source line SL in a sequence of the A state, the B state, and the C state is increased. Hence, there is a probability that the floating amount of the voltage of the source line which is generated by the current Itotal is increased together with rising of the verification level.

[0217]

The source current Itotal in the verification stage DC of the C state is more than the current Itotal in the verification stage DA of the A state. For this reason, the correction voltage VSRCx-c in the verification stage DC of the C state offsets an increased amount of the voltage that is generated by the current Itotal, and thus, the correction voltage VSRCx-c in the verification stage DC of the C state becomes lower than the correction voltage VSRCx-c in the verification stage DA of the A state.

The correction voltage VSRCx-b in the verification stage DB of the B state is, for example, equal to or higher than the correction voltage VSRCx-a, and equal to or lower than the correction voltage VSRCx-c.

[0218]

No lock out processing is applied to the flash memory according to the present embodiment, and thus the flash memory can speed up the determination processing of the threshold voltage of the memory cell MC.

[0219]

The flash memory according to the present embodiment easily performs the no lock out processing that is generated by the relatively much current Itotal, because the source line voltage is controlled based on the monitoring results of the current Itotal flowing through the source line.

[0220]

As described above, the flash memory according to the third embodiment obtains the same effect as the flash memory according to the first and second embodiments.

[0221]

(4) Fourth Embodiment

A semiconductor memory device according to a fourth embodiment will be described with reference to FIG. 15.

[0222]

The flash memory according to the fourth embodiment is different from the flash memories according to the first to third embodiments in that the no lock out processing and the lock out processing exist together at the time of determining the threshold voltage of the memory cell.

[0223]

For example, the flash memory 201 performs a writing sequence (writing loop) which uses a first program format.

[0224]

A first program format is an operation of determining the threshold voltage of the memory cell MC, using two verification level, with regard to the program verification of a certain state.

Hereinafter, the first program format is referred to as quick pass write (QPW).

[0225]

The flash memory to which the QPW format is applied sets determination levels VAVL and VBVL for QPW, in addition to the target determination levels VAV and VBV, in the A and B states. Hereinafter, for the sake of clarification of description, the determination levels VAB, VBV and VCV are referred to as target levels, and the determination levels for QPW VAVL and VBVL are referred to as QPL levels.

In the A and B state, the QPW levels (voltage values) VAVL and VBVL are lower than the target levels (voltage values) VAV and VBV, and are higher than the reading levels VA and VB.

[0226]

As illustrated in a timing chart (figure illustrating changes of potentials of each wire) of FIG. 15, in the verification stage DA of the A state, after the monitoring period and the sensing period in the verification using the QPW level VAVL, the flash memory 201 changes the verification level to the target level VAV from the QPW level VAVL. In this case, the flash memory 201 control the voltage of the bit line BL, using the no lock out processing.

In a state in which all the bit lines BL are charged, verification using the target level VAV is performed.

[0227]

According to this, verification results of the QPW level and verification results of the target level are obtained with regard to the A state.

[0228]

Even in the verification stage DB of the B state, the flash memory 201 controls the voltage of the bit line BL, in the no lock out processing, when the verification level is transitioned from the QPW level VBVL to the target level VAV.

[0229]

In flash memory according to the present embodiment, when the verification stage is transitioned from the A state to the B state, and when the verification stage is transitioned from the B state to the C state, the flash memory 201 performs the no lock out processing LCK. According to this, the sense amplifier circuit 13 sets the bit line connected to the memory cell of passed verification with regard to a certain state to a discharged state (an applied state of the source line voltages VSRC and VSRCz).

In the same manner as in the present embodiment, when presence and absence of the lock out processing exist together at the time of verification, a voltage value at the time of sensing of each state has the following values.

[0230]

In the verification stage DA of the A state, during the no lock out processing, when the verification level is transitioned from the QPW level to the target level, a current amount that is supplied to the source line at the time of verification level VAV (>VAVL) is more than a current amount that is supplied to the source line at the time of QPW level.

[0231]

For this reason, a correction voltage VSRCz-a2 of the source line voltage CELSRC in the target level VAV is equal to or lower than the correction voltage VSRCz-a1 of the source line voltage CELSRC in the QPW level VAVL.

In the same reason as at the time of verification of the A state, in the verification stage DB of the B state, a correction voltage VSRCz-b2 of the source line voltage CELSRC in the target level VBV is equal to or lower than the correction voltage VSRCz-b2 of the source line voltage CELSRC in the QPW level VBVL.

[0232]

When the verification stage is transitioned from the A state to the B state, the lock out processing is performed, and thus the current amount of the current Itotal flowing through the source line is reduced. As the result, the floating of the voltage of the source line is relaxed, and thus a correction voltage VSRCz-b1 in the QPW level VBVL of the B state is higher than the correction voltage VSRCz-a2 in the target level VAV Of the A state.

[0233]

In the same reason as this, when the verification stage is transitioned from the B state to the C state, the lock out processing is performed, a correction voltage VSRCz-c of the C state is higher than the correction voltage VSRCz-b2 in the target level VBV Of the B state.

[0234]

As described in the present embodiment, even when the threshold voltage of the memory cell is determined in such a manner that presence and absence of the lock out processing exist together, the source line control circuit 14 controls the voltage of the source line SL, based on the monitoring results of the current Itotal flowing through the source line.

[0235]

Thus, the flash memory according to the present embodiment can obtain the same effect as the first to third embodiments.

[0236]

(5) Fifth Embodiment

A semiconductor memory device according to a fifth embodiment will be described with reference to FIG. 16 and FIG. 17.

[0237]

In the flash memory according to the fifth embodiment, a source line control circuit monitors a voltage (drive voltage) VHSA that is applied to a sense amplifier circuit. The source line control circuit controls a voltage of the source line SL, based on monitoring results of the voltage VHSA on the sense amplifier circuit side.

[0238]

As illustrated in FIG. 16, a sense amplifier circuit 13 includes a regulator circuit 139. The regulator circuit 139 controls a magnitude of the voltage VHSA.

[0239]

In the flash memory according to the present embodiment, a source line control circuit 14X includes a circuit (hereinafter, referred to as a monitoring circuit) 149 for monitoring the drive voltage VHSA of the sense amplifier circuit 13 (sense unit 131). The monitoring circuit 149 may be a configuration element of the sense amplifier circuit 13.

[0240]

As illustrated in FIG. 17, the regulator circuit 139 includes an amplifier (for example, a differential amplifier) A2, a plurality of transistors TA to TD, and a plurality of resistor elements RA to RC.

[0241]

The reference voltage VREF is supplied to an input terminal (for example, inverting input terminal) ITA of the amplifier A2. A junction of two resistor elements RA and RB is connected to an input terminal (for example, a non-inverting input terminal) ITB of the amplifier A2. An output terminal OTA of the amplifier A2 is connected to a gate of the transistor (p type transistor) TA.

[0242]

One terminal of the transistor TA is connected to a voltage terminal VEXT. The other terminal of the transistor TA is connected to an output node NDA. The voltage VHSA is output from the output node NDA to a sense unit 131. The other terminal of the transistor TA is connected to a ground terminal VSS via the two resistor elements RA and RB.

[0243]

The resistor elements RA and RB function as a monitoring unit with respect to the voltage VHSA.

[0244]

The transistor TA operates in response to an output (voltage value) from the amplifier A2. According to this, a magnitude of the voltage VHSA is adjusted so as to be constant.

[0245]

The monitoring circuit 149 includes a plurality of transistors TB, TC, and TD, and a resistor RC.

[0246]

A gate of the transistor (p type transistor) TB is connected to an output terminal OTA of the amplifier A2. One terminal of the transistor TB is connected to the voltage terminal VEXT (VCC). The other terminal of the transistor TB is connected to on terminal of the transistor TC.

[0247]

One terminal of the transistor TC is connected to a gate of the transistor TA. The other terminal of the transistor TC is connected to the ground terminal VSS. A gate of the transistor TC is connected to a gate of the transistor TD.

[0248]

One terminal of the transistor TD is connected to one terminal (an output node of the regulator circuit 142) of a transistor T5. The other terminal of the transistor TD is connected to the ground terminal VSS.

[0249]

The transistor TB makes a mirror current Imrz corresponding to a drain current of the transistor TA. For example, a gate size of the transistor TB is smaller than a gate size of the transistor TA. Hence, the mirror current Imrz of the transistor TB is smaller than the drain current of the transistor TA, in proportion to the gate sizes of the two transistors TA and TB.

[0250]

The transistors TC and TD operate according to a voltage that is generated by a magnitude of the mirror current Imrz and the resistor element RC. A magnitude of an output (correction voltage value) VSRCz of the replica circuit 142 is changed depending on drain currents of the transistors TC and TD.

[0251]

For example, when much mirror current Imrz flows through the resistor element RC, gate voltages of the transistors TC and TD increase. Hence, the transistors TC and TD strongly pull currents, and thereby a current flowing through the replica elements RRP and RT increases. According to this, an amount of current drop of the replica elements RRP and RT is increased, and the correction voltage (voltage of the node ND1) VSRCz decreases.

[0252]

In contrast to this, when small mirror current Imrz flows through the resistor element RC, the transistors TC and TD weakly pull the currents. In this case, an amount of current drop of the replica elements RRP and RT is decreased. Hence the correction voltage VSRCz in a case in which the mirror current Imrz is small is higher than the correction voltage VSRCz in a case in which the mirror current Imrz is much.

[0253]

Meanwhile, when the voltage VHSA is equal to or lower than the reference voltage VERF, the drain currents (mirror current) of the transistors TA and TB increase. When the voltage VHSA is higher than the reference voltage VERF, the drain currents of the transistors TA and TB decrease.

[0254]

Adjustment of the output of the replica circuit according to an increase or a decrease of the mirror current Imrz on the sense amplifier circuit side, is repeatedly performed during the monitoring period.

[0255]

As described above, in the flash memory 201 according to the present embodiment, a change amount of the drive voltage VHSA of the sense amplifier circuit 13 side, in addition to an amount of drop of the voltage that is generated by a parasitic resistance in the memory cell array according to the replica circuit 142, is reflected to the control of the voltage of the source line.

[0256]

According to this, the flash memory according to the present embodiment can control the voltage of the source line, with a higher accuracy.

[0257]

Meanwhile, since description on the whole operations of the source line control circuit according to the present embodiment is substantially the same as the description in the first to fourth embodiments, the description thereof will be omitted herein.

[0258]

As described above, the semiconductor memory device according to the fifth embodiment obtains the same effect as the first to fourth embodiments.

[0259]

(6) Others

A read operation of a multi-value flash memory includes the following determination voltage.

[0260]

A determination voltage that is applied to a word line selected in a read operation of an A level is, for example, a voltage between 0 V and 0.55 V. However, the determination voltage of the A level is not limited to this, and may be in any one of ranges between 0.1 V and 0.24 V, between 0.21 V and 0.31 V, between 0.31 V and 0.4 V, between 0.4 V and 0.5 V, and between 0.5 V and 0.55 V.

[0261]

A determination voltage that is applied to a word line selected in a read operation of a B level is, for example, a voltage between 1.5 V and 2.3 V. However, the determination voltage of the B level is not limited to this, and may be in any one of ranges between 1.65 V and 1.8 V, between 1.8 V and 1.95 V, between 1.95 V and 2.1 V, and between 2.1 V and 2.3 V.

[0262]

A determination voltage that is applied to a word line selected in a read operation of a C level is, for example, a voltage between 3.0 V and 4.0 V. However, the determination voltage of the C level is not limited to this, and may be in any one of ranges between 3.0 V and 3.2 V, between 3.2 V and 3.4 V, between 3.4 V and 3.5 V, between 3.5 V and 3.6 V, and between 3.6 V and 4.0 V.

[0263]

Meanwhile, a period (tR) of a read operation may be any one of periods, for example, 25 ms to 38 ms, 38 ms to 70 ms, and 70 ms to 80 ms.

[0264]

A write operation of a multi-value flash memory includes a program operation and a verification operation.

[0265]

In the write operation of the multi-value flash memory, a voltage that is firstly applied to a word line selected at the time of the program operation is, for example, a voltage between 13.7 V and 14.3 V. The voltage is not limited to this value, and may be one of voltages in ranges, for example, between 13.7 V and 14.0 V, and between 14.0 V and 14.6 V.

[0266]

A voltage that is firstly applied to a word line selected when a write operation with respect to the memory cell of an odd-numbered word line is performed may be different from a voltage that is firstly applied to a word line selected when the write operation with respect to the memory cell of an even-numbered word line is performed.

[0267]

When the program operation is an incremental step pulse program (ISPP) method, a step-up voltage is, for example, approximately 0.5 V.

[0268]

A non-select voltage (pass voltage) that is applied to a non-selected word line is, for example, a value in a range between 6.0 V and 7.3 V. However, the non-select voltage is not limited to this value, may be a value in a range, for example, between 7.3 V and 8.4 V, and may be a value equal to or lower than 6.0 V.

[0269]

A pass voltage to be applied may be changed depending on whether the non-selected word line is an odd-numbered word line or an even-numbered word line.

[0270]

The time (tProg) of the write operation may be any one of periods, for example, 1700 ms to 1800 ms, 1800 ms to 1900 ms, and 1900 ms to 2000 ms.

[0271]

An erase operation of the multi-value flash memory is formed on an upper portion of the semiconductor substrate, and a voltage that is firstly applied to the well region over which the memory cell is disposed is, for example, a value in a range between 12 V and 13.6 V. The voltage is not limited to this value, and may be in any one of the values in ranges, for example, between 13.6 V and 14.8 V, between 14.8 V and 19.0 V, between 19.0 V and 19.8 V, and between 19.8 V and 21 V.

[0272]

The time of the erase operation may be any one of periods, for example, 3000 ms to 4000 ms, 4000 ms to 5000 ms, and 5000 ms to 9000 ms.

[0273]

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cells that is stacked on a substrate;

a plurality of word lines that is connected to gates of the plurality of memory cells; and

a source line that is connected to one terminal of each of the plurality of memory cells,

wherein a first voltage and a second voltage are sequentially applied to a selected word line, at the time of a read operation of data,

wherein a period in which the first voltage is applied includes a first period and a second period,

wherein a third voltage is applied to the source line during the first period and a fourth voltage is applied to the source line during the second period,

wherein a period in which the second voltage is applied includes a third period and a fourth period, and

wherein the third voltage is applied to the source line during the third period and a fifth voltage is applied to the source line during the fourth period.

2. The device according to Claim 1, wherein the fourth voltage and the fifth voltage are different from each other.

3. The device according to Claim 1 or 2, wherein the third voltage is lower than the fourth voltage.

4. The device according to any one of Claims 1 to 3, further comprising:

a first circuit that controls a voltage which is applied to the source line,

wherein the first circuit includes

a second circuit having a first resistance value corresponding to resistance components of the plurality of memory cells; and

a third circuit that controls a magnitude of an output of the second circuit as the fourth and fifth voltages, based on a first current flowing through the source line.

5. The device according to Claim 4,

wherein the first circuit includes a first transistor to which the first current is supplied,

wherein the third circuit includes a second transistor that supplies a second current corresponding to the first current to the second circuit, and

wherein a gate of the first transistor is connected to a gate of the second transistor, and a gate size of the second transistor is smaller than a gate size of the first transistor.

ABSTRACT

Drawings

FIG. 1

99: HOST DEVICE

FIG. 4

X DIRECTION

Y DIRECTION

FIG. 5

X DIRECTION

Y DIRECTION

FIG. 9

MEMORY CONTROLLER

ST100: TRANSMISSION OF WRITE COMMAND AND DATA

ST109: RECEIVE NOTIFICATION

END

FLASH MEMORY

ST0: RECEPTION OF WRITE COMMAND à START WRITING OF DATA

ST1: APPLICATION OF PROGRAM VOLTAGE

ST2: START OF PROGRAM VERIFICATION à APPLY VOLTAGE TO WORD LINE, BIT LINE, AND SOURCE LINE

ST3: MONITOR CURRENT FLOWING THROUGH SOURCE LINE

ST4: DETERMINE CORRECTION VOLTAGE TO WHICH RESISTANCE COMPONENTS OF NAND STRING IS REFLECTED, BASED ON MONITORING RESULTS OF CURRENT à CHANGE FROM REFERENCE VOLTAGE TO CORRECTION VOLTAGE à CONTROL VOLTAGE OF SOURCE LINE, USING CORRECTION VOLTAGE

ST5: SENSE VOLTAGE OF BIT LINE à RECEIVE DETERMINATION RESULTS

ST6: IS VERIFICATION PASSED?

ST7: NOTIFY END OF DATA WRITING

FIG. 10

SELECTED WL

TIME

FIG. 11

SELECTED WL

TIME

FIG. 12

TIME

FIG. 13

170(17): GENERATION UNIT

FIG. 14

SELECTED WL

TIME

FIG. 15

SELECTED WL

FIG. 16

139(13): REGULATOR CIRCUIT